Amendments to the Claims

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1.-14. (Cancelled)

15. (Currently Amended) A method for setting up a program-controlled circuit arrangement with a processor unit, an assigned non-volatile start procedure memory and an interface for connection to a data transmission network, whereby the processor unit is set up in such a way that, after being switched on, it executes a start procedure stored in the start procedure memory, wherein a start procedure is stored in the start procedure memory, wherein the start procedure is set up in such a way that during its execution the processor unit connects up by means of the interface to an operating program server and from this loads operating program instructions into a main memory assigned to the processor unit; wherein the start procedure is set up in such a way that during its execution the processor unit loads and executes a download procedure from a non-volatile download procedure memory into the main memory, and the download procedure is set up in such a way that during its execution the processor unit connects up by means of the interface to the operating program server and from this loads operating program instructions into the main memory assigned to the processor unit; and wherein the main memory storing the download procedure is separate from the start procedure memory but part of the programmed-controlled circuit.

16 . (Canceled)

17. (Previously Presented) The method of claim 15, wherein the circuit arrangement has an exchange arrangement for exchanging data packets within the data transmission network.

18. (Currently Amended) The method of claim 15, ~~characterized in that~~ wherein the circuit arrangement is a circuit for providing a telephone and/or fax service via the data transmission network.

19. (Currently Amended) The method of claim 15, ~~characterized in that~~ wherein the start procedure memory is integrated with the processor unit on a semiconductor module.

20. (Previously Presented) The method of claim 15, wherein the download procedure memory and the processor unit are integrated in various semiconductor modules and the download procedure is loaded serially from the download procedure memory.

21. (Previously Presented) The method of claim 20, wherein the download procedure memory (4) is a serial EEPROM.

22. (Currently Amended) A circuit arrangement with a processor unit, an assigned non-volatile start procedure memory and an interface for connection to a data transmission network, whereby the processor unit is set up in such a way that it executes a start procedure stored in the start procedure memory after being switched on, wherein a start procedure is stored in the start procedure memory, wherein ~~said~~ the start procedure is set up in such a way that during its execution the processor unit connects up by means of the interface to an operating program server and from this loads operating program instructions into a main memory assigned to the processor unit; wherein the start procedure is set up in such a way that during its execution the processor unit loads and executes a download procedure from a non-volatile download memory, which is connected to the processor unit, into the main memory, whereby the download procedure is set up in such a way that during its execution the processor unit connects up by means of the interface to the operating program server and from this loads operating program instructions into the main memory assigned to the processor unit; and wherein the main memory storing the download procedure is separate from the start procedure memory but part of the programmed-controlled circuit .

23. (Canceled)

24. (Previously Presented) The circuit arrangement of claim 22, wherein the circuit

arrangement has an exchange arrangement for exchanging data packets within the data transmission network.

25. (Previously Presented) The circuit arrangement of claim 22, wherein the circuit arrangement is a circuit for providing a telephone and/or fax service via the data transmission network.

26. (Previously Presented) The circuit arrangement of claim 22, wherein the start procedure memory is integrated with the processor unit on a semiconductor module.

27. (Previously Presented) The circuit arrangement of claim 22, wherein the download procedure memory and the processor unit are integrated in various semiconductor modules and the download procedure memory has a serial output for the download procedure.

28. (Previously Presented) The circuit arrangement of claim 27, wherein the download procedure memory is a serial EEPROM.